SEMICONDUCTOR DEVICE AND METHOD FOR MAKING THE DEVICE HAVING AN ELECTRICALLY MODULATED CONDUCTION CHANNEL

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BACKGROUND OF THE INVENTION

The present invention relates to the MOS semiconductor art. Specifically, a semiconductor device having an electrically controllable channel width is described which may be used in applications where matching the electrical parameters of devices on a single integrated circuit is desirable.

Integrated circuits having MOS derived components have manufacturing tolerances which vary with position on the device, and transistors located on one portion of a semiconductor substrate may have different gain characteristics than those in other locations on the substrate. Variations in the device characteristics across the integrated circuit result from random and systematic variations in manufacturing processes. The process variations include photolithographic image size variations, etch image size variations, ion implant dopant level variations and the thickness of deposited or grown films. These variations become increasingly significant as the area of the devices decreases.

Some electronic circuit applications require that the transistors have an essentially matched gain. One such application is a digital to analog converter, wherein a ladder network is provided generating a plurality of reference currents from a constant reference current distributed throughout the integrated circuit. A designer will provide for a single source of current as the reference value, and the value of the reference current is reproduced in locations throughout the integrated circuit. Variations in transistor gain across the integrated circuit will result in random and systematic variations in reference currents which are replicated throughout the device.

The present invention has been derived to provide semiconductor devices, such as a transistor or a resistor, having electrical properties which can be matched to other similar devices located on the substrate.

SUMMARY OF THE INVENTION

The present invention provides for a semiconductor device having an electrically modulated conduction channel. The device is located within a trench structure formed in a substrate of an MOS integrated circuit, and a diffusion region within the trench structure is electrically modulated by applying a voltage between the trench and substrate.

In accordance with one embodiment of the invention, the device located within the trench structure may be an FET transistor, having a gate deposited over the diffusion region. The channel width below the gate can therefore be modulated by applying an electrical potential between the trench structure and the substrate, producing a change in the transistor gain. Accordingly, the gain of the device may be effectively set by varying the voltage potential between the trench structure and the substrate to match the gain of other transistors on the substrate.

In accordance with the invention, a pair of transistors having similar characteristics may be formed within the trench. If a known gain is established in one of the transistors, by controlling the trench to substrate potential, so that a known current flows therethrough, the gain on the other transistor is commonly controlled by the same potential between the trench and substrate, and the other transistor can be used to generate a reference current. Different pairs of transistors located in other trenches on the substrate may be set to the same gain, if the known current is set in one of the transistors. The remaining transistor of each pair of transistors in a trench may be advantageously used to generate the same reference current if their gate connections are commonly connected.

In yet another embodiment of the invention, the trench structure may include multiple diffusion regions which serve as resistor controlled from a common control voltage.

In still another embodiment of the invention, each diffusion region is surrounded by a single trench structure which controls the diffusion region.

DESCRIPTION OF THE DRAWINGS

Figure 1A is a plan view of a channel modulated FET transistor in accordance with the preferred embodiment;

Figure 1B illustrates a section view of the transistor of Figure 1A;

Figure 1C illustrates the effect of applying positive potential between the trench and substrate;

Figure 1D illustrates the effect of applying a negative potential between the trench and the substrate;

Figure 2 illustrates an application for controlling the gain of one of a pair of transistor devices in accordance with the preferred embodiment;

Figure 3 is a schematic illustration of the circuit of Figure 2;

Figure 4 illustrates another embodiment of the invention for matching the value of resistors at different locations on the substrate;

Figure 5 is a top view of one of the resistor banks of the device of Figure 4;

Figure 6A is a section view of the device of Figure 5 along lines A-A;

Figure 6B is a second section view along lines B-B of the resistor bank of Figure 5;

Figure 7 represents a prior art digital-to-analog converter which may be improved utilizing one embodiment of the invention;

Figure 8 illustrates an improved digital-to-analog converter which converts a voltage output to a current output having a high linearity; and

Figure 9 illustrates an improved digital-to-analog converter having current sources which are channel modulated to improve the linearity.

DESCRIPTION OF THE PREFERRED EMBODIMENT

A transistor having an electrically modulated channel in accordance with the present invention is shown more particularly in Figures 1A through 1D. Referring now to Figures 1A through 1D, a trench structure 12 is shown formed in an integrated circuit substrate. The trench has a depth D of approximately .3 to .4μ. A connection 21 is formed on the trench, to which a voltage may be applied, and a similar connection 22 is provided on the substrate 25. A diffusion region 11 is formed in the substrate, surrounded by the trench, and a gate 18 is formed over the diffusion region 11. Source and drain regions are provided on either side of the gate 18 to form a transistor.

As illustrated in Figures 1B-1D, the trench is filled with a polysilicon material 26 and includes a thin oxide layer along the inner and outer side walls. The electric field created between the trench and substrate modulates the channel width as shown in Figures 1C and 1D. In response to the application of a positive potential between terminals 21 and 22, a thin $P^=$ layer forms at the trench body interface, and the gate will have a greater effective width than with no potential applied. As shown in Figure 1D, when a negative voltage potential is applied between the trench contact 21 and substrate 22, a thin P^+ layer forms at the trench body interface, effectively narrowing the width of the gate, and the channel underneath the gate.

The narrowing width does not effect the threshold for the transistor, if the transistor width is above a predetermined factor. Control over channel width, in turn, provides a direct control over the gain (g_m) of the device.

An application for the electrically modulated transistor which provides a controlled reference current at various points within the integrated circuit is shown in Figures 2 and 3. Figure 2 illustrates a basic building block for providing transistors having matched gains in different portions of the integrated circuit substrate. Q2′ and Q3′, as well as Q1′, are located on a different portion of the integrated circuit substrate than Q1, Q2 and Q3. However, both circuits are capable of generating the identical current through Q3 and Q3′ by establishing

the identical gain for Q3 and Q3′ and a common gate to source voltage, even though the transistors may not be matched at the time of manufacture.

The circuit of Figure 3 takes advantage of the fact that because Q1 and Q1′ occupy a large area of the substrate, their gain characteristics (g_m) are more closely matched, as the degree of mismatched generally proportional to:

$$\frac{1}{\sqrt{A}}$$

where A is the area of the transistor on the substrate. Q1 and Q1′ have gates connected to the same reference voltage 42, which may be Vdd/2, and identical currents are established through Q1′, Q1 and the serial connection of Q2′ and Q2. The trench containing Q2 and Q3 is modulated with the drain voltage of Q1, so that Q2 assumes a gain value sufficient to support a current determined by the reference voltage 42 on the gate connection of Q1 and Q1′. While Q2 and Q2′ may not be matched, their gains will be set to be the same in order to derive the same source-drain current through Q1′, Q2′, and Q1 and Q2. Process variations between Q2 and Q3 are minimal, even though the devices have a much smaller area on the substrate than Q1. Once the gain of Q2 is fixed, the gain of Q3 which because of its proximity to Q2 is substantially the same as Q2, is also fixed.

Figure 2 shows the general configuration where the two transistors, Q2 and Q3, are included within the diffusion area 11. Each of the transistors includes a gate 18, 180, as well as a source drain region 17-19 within the diffusion area 11. The current source 35 carrying the reference current connects to the drain of Q3. The source of Q2 and Q3 is connected to the common ground 32. Each of the nFETs Q2 and Q3 are controlled by a current from Q1, which is a pFET within an N well 36. The drain of Q1 is connected to the drain of Q2, through terminal 33, as well as to the trench 12. Current flowing through Q1 is established by the reference voltage connected to terminal 42, and the gain of Q1 establishes a voltage

on the trench which in turn sets the gain of Q2 sufficient to carry the current of Q1. As illustrated in Figure 3, the trench is effectively a capacitor, coupling the same electrostatic charge across a conduction channel, thereby setting the same gain for Q2 and Q3.

The illustrated circuit of Figure 3, duplicating the device is Q3′, Q2′ and Q1′, permits the identical current of current source 35 to be established in RL. As Q1′ has a large area equal to the area of Q1, it has substantially the same gain as Q1, and the same current is established for Q1′. This, in turn, sets the gain of Q2′ to be the same as Q2 by changing the trench voltage to compensate for process variation. Because of Q2′ proximity to Q3′, it establishes the same gain for Q3′ which has a gate to source voltage the same as Q3. Accordingly, RL must carry the same drain source current as current source 35 provides.

It is also possible to include more than two transistors in a trench which will permit other circuits to be implemented which need transistors having matching gains.

The foregoing circuit permits the duplication of a reference current 35 in numerous places in the integrated circuit by establishing a large area transistor such as Q1 and Q1′ in each location which will have the same gain, and carry the same current, given the fact that larger area transistors are already matched. Connecting one of the two transistors within a trench in series with one of the larger transistors, so that the series connected transistors carry the same current, will establish the same gain for the remaining transistor in the trench. The current through each of the drain source circuit of the remaining transistor in each trench will be the same when the gates of these transistors are connected together.

The foregoing principles may also be applied to control devices which are not field effect transistors. For instance, Figure 4 illustrates a circuit which matches the resistance values in one location of the substrate to resistance values at another location on the substrate. Due to the aforesaid process variations during the manufacture of the integrated circuit, the resistor values may not be well matched. The implementation according to Figure 4 permits a trimming of the value by changing an electrical potential associated with

resistors on one portion of the substrate with respect to an electrical potential of another portion of the substrate containing another set of resistors.

Referring now specifically to Figure 4, a bank of resistors 50-54 are shown which are located on a different portion of the circuit substrate than resistors 65-69. Each bank of resistors 50-54, 65-69 are located within a trench 56, 71 of a substrate. The trench walls which enclose each of the resistor banks are connected via a respective connection 63, 70 to the output of the first and second differential amplifiers 48, 49. Differential amplifiers 48 and 49 provide a potential for modulating the width of the resistors of a respective resistor bank. Thus, where the resistors of those banks are to be matched with respect to each other, i.e., resistor 50 = 69, 56 = 68, 51 = 67, . . . a control voltage may be derived for modulating the width of each of the resistors of a resistor bank.

In the circuit of Figure 4 the resistance of R1 is set equal to the resistance R2 and R3 is set equal to R4, by virtue of the fact that differential amplifiers 48 and 49 will assume output values which produce 0 volts between the inverting and non-inverting inputs of amplifiers 48 and 49. The potential applied to the trench walls produces an electrostatic field between the walls of trenches 56, 69 and the substrate 72, effectively modifying the width and resistance value of the resistors within a trench.

Figures 5, 6A and 6B show in greater detail the construction of a given trench 56 and the individual resistors within the trench. Referring now to Figures 5, 6A and 6B, the resistors comprise a diffusion layer 59, shown as doped N+, formed within a well of polysilicon 60 deposited within the trench 56. The diffusion 59 is connected to contacts 61 and 64, formed through an oxide layer 60. Contacts 61 and 64 provide for connections to the resistor.

The trench is filled with polysilicon, and each of the resistors 50-54 are separated from the trench by a thin oxide layer shown as 50a for resistor 50. Accordingly, a potential applied between terminal 63 and the substrate 72 provides an electrostatic field for modulating the width of each resistor of a bank. Thus, the two banks of resistors have

matched pairs of resistors at different locations on the substrate. As shown in Figure 6B, changes in the trench voltage deplete the N+ region near the trench walls, increasing the resistance of each resistor.

The foregoing embodiments utilize isolation trenches which are in use in semiconductor manufacturing processes. Formation of shallow isolation trenches throughout the substrate permit the creation of actively controlled components such as the foregoing. In those instances where the components are not to be controlled, the trench walls may be tied to the same potential as the substrate.

The process of forming such shallow isolation trenches are conventional, and well known. Such devices are currently used as capacitors, and for other applications where isolation of one component from another is necessary.

A transistor having an electrically modulated channel is useful in digital-to-analog converters. A prior art digital-to-analog converter (DAC) is shown more particularly in Figure 7. The device of Figure 7 includes a digital decoder 74, which creates pairs of control signals for each digit of an input signal. The pairs of control signals control current flow in one or the other transistor of a current branch. Each current branch includes a current source, operated in saturation at a value which is weighted according to the order of an applied digit, which supplies current through first or second transistors and converts the bit into a current supplied to output 88. The lowest order bit controls transistors 80, 81 to supply current from current source transistor 75. Higher order bits are represented by the current flow in the current branch including source 76, transistors 82 and 83, and the current flow in the branch including current source 77, and transistors 84 and 85. The current source transistors 75, 76 and 77, are all driven by a common analog bias voltage applied to common gates 89. Depending upon the digital value and its complement, current is either directed to the output 88 or to ground. Shunting current which is not directed to the output 88 to ground provides a reduction in unwanted transients, when switching current to the output 88 through one of the transistors 80, 82 or 84.

The accuracy of the device depends in part on the ability to generate a known and precise current through each branch from current sources 75, 76 and 77. Typically, this is realized by having transistors 75, 76 and 77 quite wide, making their width (w) proportional to the value of current needed in the respective branch. The unfortunate consequence is the use of a large amount of chip area. Additionally, due to process variations, the transistors 75, 76 and 77 produce a variation in currents which reduce the linearity of the output.

The transistor having an electrically modulated channel may be useful in digital-to-analog to converter circuits for reducing the spread in current source gains, and the resulting decrease in DAC linearity, linearity being a measure of the output value with certainty, given a known digital input as determined across the digital input range.

One approach of using the device in accordance with the invention is shown in Figure 8. A digital signal is decoded in a digital decoder 74 and used to derive an output voltage. The devices 90, 91 and 92 comprise a low power voltage DAC. The low power voltage DAC, known to those skilled in the art, creates an output voltage which in some applications needs to be converted to a current. The lower power voltage DAC charges a capacitor bank 91 to a voltage proportional to the input digital signal. A charge stored on the capacitor bank 91 is integrated in an integrator 92, and the value is sampled and held in the sample/hold circuit 93 while charge/integration takes place.

The low power voltage DAC utilizes less chip area than the device of Figure 7, even when the voltage to current converter using a transistor having a modulated channel width is employed. The voltage output from the low power voltage DAC 90 modulates the width of transistors 75a and 80a. An output node 88a provides the current which is proportional to the voltage applied to the trench connection 94.

The result is a current output which, with proper centering of the trench bias, provides a current which oscillates around the current value set by the DC voltage component on trench contact 94. The voltage to current converter 90 provides a current midpoint, reducing thermal and electromigration as well as an improvement in power consumption over the prior

art device in Figure 7. The disadvantages of the circuit of Figure 8, however, include its inability to produce a 0 current at its output, and a reduced high frequency capability due to the fact that the system relies upon the charge and discharge of a capacitor bank 91.

Figure 9 represents a more advantageous application of a trench modulated transistor in accordance with the present invention in a DAC. As shown in Figure 9, each of the current sources includes a transistor 75, 76 and 77, having its own trench bias voltage. By applying an individual trench bias to each of transistors 75, 76 and 77, it is possible to compensate for manufacturing tolerances which produce transistors having a width deviating from the desired width. Thus, the current through each of the branches may be advantageously trimmed by controlling the trench bias produced by bias network 100. The bias voltage may be controlled using laser trimming, or through a fuse blow or other known techniques for changing the value of a bias network connected to a source of bias voltage or using a biasing circuit such as shown in Figures 2 and 3.

The foregoing description of the invention illustrates and describes the present invention. Additionally, the disclosure shows and describes only the preferred embodiments of the invention, but as aforementioned, it is to be understood that the invention is capable of use in various other combinations, modifications, and environments and is capable of changes or modifications within the scope of the inventive concept as expressed herein, commensurate with the above teachings, and/or the skill or knowledge of the relevant art. The embodiments described hereinabove are further intended to explain best modes known of practicing the invention and to enable others skilled in the art to utilize the invention in such, or other, embodiments and with the various modifications required by the particular applications or uses of the invention. Accordingly, the description is not intended to limit the invention to the form disclosed herein. Also, it is intended that the appended claims be construed to include alternative embodiments.